DANIEL R. MERCER

STAFF ASIC DESIGN ENGINEER · CPU & GPU MEMORY SUBSYSTEMS

Santa Clara, CA · (408) 555-0142 · daniel.mercer@example.com · LinkedIn

PROFILE

ASIC design engineer with 10+ years taking high-performance CPU and GPU logic from micro-architecture to production silicon. Owns RTL, timing closure and power for cache and memory-subsystem blocks on 5 nm and 7 nm nodes, and has led teams of up to six engineers through four first-pass tape-outs.

CORE EXPERTISE

- Micro-architecture & RTL
- Caches & memory controllers
- Pipelining & retiming
- Static timing analysis
- Synthesis & equivalence
- Post-silicon debug
- Low-power design (UPF)
- CDC / RDC sign-off
- Technical leadership

PROFESSIONAL EXPERIENCE

NVIDIA — Santa Clara, CA

Staff ASIC Design Engineer — GPU Memory Subsystem — Jun 2022 – Present

- Lead micro-architecture and RTL for the **L2-cache request arbiter** of a data-center GPU (5 nm): wrote the spec, split the work across a six-engineer team and delivered **first-pass silicon**.
- Cut the arbiter's critical path by **18%** by re-pipelining tag compare and retiming hazard checks, closing timing at **1.9 GHz** with no added load-to-use latency.
- Reduced block dynamic power by **22%** through fine-grained clock gating driven by activity-based analysis; the flow was adopted by three sister teams.
- Built the block's CDC/RDC sign-off flow, shrinking late-stage waivers from ~140 to **12**; mentor four engineers and run the weekly timing-triage review.

Senior ASIC Design Engineer — DRAM Controller — Mar 2020 – Jun 2022

- Owned RTL for the memory-controller command scheduler (7 nm); bank-aware request reordering raised effective DRAM bandwidth by **9%** on target workloads.
- Worked with verification to reach 100% functional-coverage closure **two weeks ahead** of RTL freeze; fixed 30+ bugs found in emulation before tape-out.

Intel Corporation — Hillsboro, OR

Component Design Engineer — CPU Core, Load/Store Unit — Jul 2015 – Feb 2020

- Designed RTL for load/store-unit components of a client CPU core, including store-to-load forwarding and a 16-entry fill buffer.
- Closed 40+ critical paths per milestone across PVT corners and delivered timing and functional ECOs through tape-out on **two product generations**.
- Root-caused a store-forwarding corner case in post-silicon using scan dumps and on-chip trace; fix shipped in a metal-only stepping.
- Wrote a Python regression-triage tool that clusters failures by signature, saving the team ~10 hours per week.

EDUCATION

M.S., Electrical & Computer Engineering — 2015
Georgia Institute of Technology — Computer Architecture & VLSI

B.S., Electrical Engineering — 2013
Purdue University — with Distinction

TECHNICAL SKILLS

LANGUAGES SystemVerilog, Verilog, Python, Tcl, Perl

IMPLEMENTATION Synopsys Fusion Compiler, PrimeTime, Formality, Spyglass

SIMULATION VCS, Verdi, Xcelium

POWER UPF, PrimePower, clock & power gating