Priya Natarajan

Senior Design Verification Engineer

CONTACT

LOCATION
Austin, TX

PHONE
(512) 555-0187

EMAIL
priya.natarajan@example.com

ONLINE
LinkedIn · GitHub

SKILLS

Verification

UVM · SVA · Formal · Constrained-random · Coverage closure · Gate-level sim

Protocols

AXI4 / ACE · CHI · APB · PCIe (basics)

Languages

SystemVerilog · C / C++ · Python · Tcl

Tools

VCS · Xcelium · Verdi · JasperGold · Palladium · Git · Jenkins

EDUCATION

M.S. Electrical & Computer Eng.
University of Illinois Urbana-Champaign
2020 · Thesis: formal checks for cache coherence

B.S. Electrical Engineering
University of Illinois Urbana-Champaign
2018 · GPA 3.7 / 4.0

SUMMARY

Design verification engineer with 6 years verifying CPU interconnect and SoC IP at Apple and AMD. I build UVM testbenches from scratch, pair simulation with formal to hunt deadlocks, and own coverage closure through tape-out — with an eye on bugs that only show up under real traffic.

140+
RTL bugs filed across three tape-outs

100%
functional coverage at every sign-off

14h → 5h
nightly regression turnaround

EXPERIENCE

Silicon Design Verification Engineer
Aug 2022 – Present

Apple · Austin, TX

Block-level verification lead for a coherent fabric in Apple silicon SoCs.

- Architected the UVM environment for the fabric: agents, scoreboard and a **coherency checker** that tracks every line's state across caches.
- Wrote **300+ SystemVerilog assertions** for protocol and forward-progress checks; formal proofs exposed **3 starvation bugs** that simulation had missed.
- Closed **100% functional** and **98% code coverage** for tape-out and filed 85 RTL bugs, six of them ordering or deadlock issues.
- Cut nightly regression from **14 h to 5 h** by bundling constrained-random tests and adding priority queues to the compute farm.
- Reproduced two post-silicon failures on emulation within a week, which unblocked the bring-up team.

ASIC Design Verification Engineer
Jul 2020 – Aug 2022

AMD · Austin, TX

Verification of DMA and interrupt IP for client APUs.

- Verified an **AXI4 DMA engine** and its interrupt controller from test plan to sign-off.
- Built reusable AXI and APB UVM agents that **four IP teams** adopted.
- Developed a C++ reference model connected over DPI-C for transaction-level scoreboard checking.
- Filed 55 RTL bugs and led gate-level simulation sign-off with SDF back-annotation.

Graduate Research Assistant
Aug 2018 – May 2020

University of Illinois Urbana-Champaign · Computer Architecture Lab

- Model-checked a directory-based MESI protocol for a 16-core research chip and found two race conditions before RTL freeze.
- Wrote a Python generator that turns protocol tables into SVA properties, cutting property-writing time by half.

LEADERSHIP & IMPACT

- **Formal deadlock kit:** packaged the fabric's liveness properties and abstraction models into a reusable kit that **two other fabric teams** now run nightly.
- **Mentoring:** onboarded three new-grad verification engineers and ran a six-session internal UVM bootcamp.
- **Process:** introduced bug-escape reviews after each tape-out; the checklist is now part of the team's sign-off template.