Ethan Caldwell

Electrical & Computer Engineering, B.S. 2026 · Digital Design & ASIC · Open to full-time roles

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3.82 GPA / 4.00

EDUCATION

The University of Texas at Austin
Aug 2022 – May 2026

Bachelor of Science, Electrical and Computer Engineering — Integrated Circuits track

Austin, TX

Digital System Design · Computer Architecture · VLSI Circuit Design · Embedded Systems · Analog ICs · Signals & Systems

Honors: University Honors (6 semesters) · Cockrell School of Engineering Scholarship

EXPERIENCE

ASIC Design Engineering Intern
May 2025 – Aug 2025

Qualcomm · San Diego, CA · Modem subsystem team

- Designed a parameterized **asynchronous FIFO** with Gray-code pointers in SystemVerilog for a clock-domain crossing; passed CDC lint with **zero waivers** and a coverage-driven testbench.
- Closed synthesis timing at **1.2 GHz** by retiming a pointer-compare path, which also cut block area by **11%**; presented results to a 20-person design team.

Student Engineer, Validation Lab
Sep 2024 – May 2026

Silicon Labs · Austin, TX · Part-time, 20 h/week alongside classes

- Automated bench characterization of wireless-SoC power modes in Python (PyVISA, SMUs, scopes), turning a two-day manual sweep into **four hours**.
- Measured sleep current on **120+ parts** across three temperatures and flagged a 15% outlier lot, which led to an updated production test limit.

PROJECTS

5-Stage Pipelined RISC-V CPU
Spring 2025

SystemVerilog · Vivado · Basys 3 FPGA

RV32I core with hazard detection, full forwarding and a static branch predictor; passes the official riscv-tests suite.

100 MHz ON FPGA · **1.18** CPI

Write-Back Cache Controller
Fall 2025

AXI4-Lite · Verilator · cocotb

4 KB direct-mapped write-back cache, verified with a Python testbench driving randomized traffic against a reference model.

4 KB CAPACITY · **95%** LINE COVERAGE

8-bit SAR ADC — Senior Design, team of 4
2025 – 2026

Cadence Virtuoso · 65 nm CMOS · Post-layout sim

Owned the dynamic comparator and capacitive DAC, from schematic through layout and extraction.

7.4 ENOB · **10 MS/s** SAMPLE RATE

SKILLS

HDL & CODE	SystemVerilog, Verilog, C, Python, MATLAB
EDA	Vivado, Verilator, cocotb, Cadence Virtuoso, Synopsys Design Compiler, LTspice
LAB	Oscilloscopes, logic analyzers, SMUs, spectrum analyzers, soldering

LEADERSHIP

Workshop Lead, IEEE UT Austin
2023 – 26

Taught weekly Verilog & FPGA workshops to **60+ students** and wrote the branch's starter lab guide.